CLAIMS

What is claimed is:

1. A method for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation, comprising:

connecting interface pins of at least two pre-diffused IP blocks in a semiconductor device to input ports of a multiplexer;

connecting an output port of said multiplexer to an I/O pin of said semiconductor device;

providing an address to said multiplexer through a configuration pin of said semiconductor device to decide which of said interface pins is actually connected to said I/O pin; and

connecting said I/O pin to a reusable field programmable device so that an IP block having said interface pin is selected for prototyping.

2. The method of claim 1, wherein said multiplexer has two input ports.

3. The method of claim 1, wherein said multiplexer has at least three input ports.

4. The method of claim 1, wherein said reusable field programmable device is a field programmable gate array.

5. The method of claim 1, wherein said reusable field programmable device is a programmable logic device.

6. An apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation, comprising:

a multiplexer;

means for connecting interface pins of at least two pre-diffused IP blocks in a semiconductor device to input ports of a multiplexer;

means for connecting an output port of said multiplexer to an I/O pin of said semiconductor device;

means for providing an address to said multiplexer through a configuration pin of said semiconductor device to decide which of said interface pins is actually connected to said I/O pin; and

means for connecting said I/O pin to a reusable field programmable device so that an IP block having said interface pin is selected for prototyping.

7. The apparatus of claim 6, wherein said multiplexer has two input ports.

8. The apparatus of claim 6, wherein said multiplexer has at least three input ports.

9. The apparatus of claim 6, wherein said reusable field programmable device is a field programmable gate array.

10. The apparatus of claim 6, wherein said reusable field programmable device is a programmable logic device.

11. An apparatus for exposing pre-diffused IP blocks in a semiconductor device for prototyping based on hardware emulation, comprising:

pre-diffused IP blocks in a semiconductor device,

I/O pins of said semiconductor device for providing input and output to said semiconductor device;

a multiplexer communicatively coupled to interface pins of said pre-diffused IP blocks and one of said I/O pins;

a configuration pin of said semiconductor device for providing an address to said multiplexer to decide which of said interface pins is connected to said I/O pin.

12. The apparatus of claim 11, wherein said semiconductor device is based on a slice.

13. The apparatus of claim 11, wherein said multiplexer has two input ports.

14. The apparatus of claim 11, wherein said multiplexer has at least three input ports.

15. The apparatus of claim 11, further comprising a reusable field programmable device connected to said I/O pin for prototyping.

16. The apparatus of claim 15, wherein said reusable field programmable device is a field programmable gate array.

17. The apparatus of claim 15, wherein said reusable field programmable device is a programmable logic device.